

FW843

IEEE® 1394b Bilingual Three-Port Cable Transceiver/Arbiter



FEATURES

- Provides three backward-compatible IEEE-1394 bilingual cable ports.
- Fully supports provisions of IEEE 1394b-2002.
- Fully supports provisions of IEEE 1394a-2000 and IEEE 1394-1995 standards.
- Supports 1394a speeds of S100, S200, and S400.
- Supports 1394b-2002 speeds of S400B and S800B.
- On-chip (PLL) for high-speed clock generation.
- Full 1394a-2000 support includes the following:
 - Connection debounce.
 - Extended resume signaling for compatibility with legacy DV (digital video) devices.
 - Arbitrated short reset.
 - Port disable/suspend/resume.
 - Multispeed concatenation.
 - Fly-by concatenation.
 - Arbitration acceleration.
- Single 3.3 V supply and on-chip 1.2 V voltage regulator.
- Low-power sleep mode.
- Powerdown modes to conserve energy for battery-operated applications.
- Fully compliant with open host controller interface (OHCI) requirements.
- Cable power sense function to detect external cable power.
- Register bits give software control of contender bit, power class bits, link active control bit, and 1394a-2000 features.
- External pin control of power-class bits.
- Data interface to link-layer mode is pin-selectable from 1394a-2000 mode or 1394b-2002 mode.
- Interoperable with other 1394 physical layers using 1.8 V, 3.3 V, and 5.0 V supplies.
- Low-jitter on-chip crystal oscillator provides transmit and receive data at 98.304 Mbits/s, 196.608 Mbits/s, 393.216 Mbits/s, 983.04 Mbits/s, and a link-layer controller clock at 49.152 MHz or 98.304 MHz.
- Fail-safe circuitry senses sudden loss of power to the device. The ports are disabled to ensure that the FW843 does not load the TPBIAS with any connected device and blocks any leakage from the port back to the power plane.
- 1394a-2000 compliant common-mode noise filter on the incoming bias detect circuit filters out crosstalk noise.
- Scan test modes.
- 84-pin MLCC package.

The FW843 provides the digital and analog functions needed to implement a three-port node in a cable-based IEEE 1394 network. All three ports are compliant with IEEE-1394b-2002 and backward-compatible with IEEE 1394a-2000 and IEEE 1394-1995. The three ports are capable of monitoring the line conditions for determining the connection status, initialization and arbitration, and for the packet reception and transmission.

Description

The FW843 provides the digital and analog functions needed to implement a three-port node in a cable-based IEEE 1394 network. Each of the three ports can be configured to work in data-strobe mode only (1394a-2000) by pulling the corresponding DSMO input pin to the 3.3 V supply.

The FW843 supports the following 1394 speeds:

- S100 (98.304 Mbits/s)
- S200 (196.608 Mbits/s)
- S400 (393.216 Mbits/s)
- S400B (491.52 Mbits/s)
- S800B (983.04 Mbits/s)



Description (Cont.)

The FW843 includes a cable power sense (CPS) function to detect external cable power. The cable interface on each port can follow either the IEEE 1394a-2000 protocol or the IEEE 1394b-2002 protocol, depending on the interface capabilities of the remote node. When a port is connected to a 1394a-2000 compliant node, the cable interface on the port works in the 1394a-2000 mode at S100, S200, or S400 speeds. When a port is connected to a 1394b-2002 compliant node, the cable interface on the port works in the 1394b-2002 mode at S400B or S800B speeds.

The FW843 requires an external crystal to drive the internal PLL (phase-locked loop), which generates high-speed clock signals needed for the transmission of serial data. An external low-jitter 24.576 MHz crystal can be connected between pins XLO and XHI when input pin ENXTAL is pulled to the 3.3 V supply. When the ENXTAL pin is pulled to ground, an external 24.576 MHz or 98.304 MHz reference clock can be connected to the XLO input pin. The

frequency of the reference clock is selected by either pulling input pin REFSEL to ground (24.576 MHz) or to the 3.3 V supply (98.304 MHz).

The PHY-LINK interface can support either the IEEE 1394a-2000 protocol or the IEEE 1394b-2002 protocol. The PHY-LINK interface mode is controlled by input pin PLIMODE. When the PLIMODE pin is asserted, the PHYLINK interface operates in the IEEE 1394b-2002 mode. The FW843 generates a 49.152 MHz clock on output pin PCLK when PLIMODE is deasserted. When PLIMODE is asserted (and LPS is asserted), a 98.304 MHz clock is generated on the PCLK output. The PCLK clock is used by the link device to synchronize data transfer between the link device and the FW843.

The FW843 receives transmit data from the link device on 2, 4, or 8 bits of the data bus, depending on the requested transmission speed and the PHY-LINK interface mode of operation. The transmit data is latched by the

FW843, serialized, and transmitted on the cable interface at the requested speed. The FW843 receives serial data on the cable interface. The received data stream is synchronized to the local clock and converted into parallel data bits. The parallel data is sent to the link device on 2, 4, or 8 bits of the data bus, depending on the mode of operation of the PHY-LINK interface.

The FW843 uses a single 3.3 V power supply and has an on-chip voltage regulator to generate the internal 1.2 V supply used by the digital core and analog circuitry.

Crystal

The FW843 is designed to use an external 24.576 MHz parallel resonant fundamental mode crystal to provide the reference for an internal oscillator circuit. The IEEE 1394a-2000 standard requires that FW843 have less than ± 100 ppm total variation from the nominal data rate, which is directly influenced by the crystal.

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